We claim:

1. A communications acquisition method, which comprises:

correlating a binary-coded spread sequence arriving at a frequency f and having m bits with a locally generated spread sequence by phase-shifting a multiplicity of locally generated spread sequences with respect to the received spread sequence;

correlating the received spread sequence with a locally generated spread sequence at the frequency f;

storing the received spread sequence and processing the stored, received spread sequence at an oversampling rate of i*f, where i is an integer; and

splitting the stored, received spread sequence into i sections and carrying out the correlation in i steps.

2. The method according to claim 1, which further comprises:

shifting the received spread sequence bit by bit within k cycles in k section variants each having m bits at an oversampling rate of k*f, where k is an integer, by shifting a most significant bit of a section variant to a position of a least significant bit of a succeeding section variant;

after k cycles, replacing the least significant bit by a succeeding bit of the received spread sequence and repeating the shifting and replacing steps (m-1) times;

subdividing the locally generated spread sequence into k sections each having n bits, where n is an integer, and comparing each of these sections with a section variant of the received spread sequence within a cycle;

counting all matches and storing the count results; and

carrying out a maximum search over all the count results.

3. The method according to claim 2, wherein a number of sections of prescribed length is k=32 and a chip length of the sections is n=32.

4. A correlator for performing a communications acquisition, comprising:

a FIFO memory having a memory input and a memory output, said FIFO memory inputting and outputting content;

a shift register with feedback for holding a received signal sequence in serial form, said shift register being clocked at an oversampling rate and having register positions connected

in parallel to said memory input for parallel storage of a plurality of shift register contents read out in succession, said memory output being connected in parallel with said register positions for parallel transfer of data to said shift register;

a further memory for holding reference signal sequences; and

a comparator for comparing the content of said FIFO memory with a content of said further memory at said oversampling rate;

the correlator programmed to perform the steps of:

correlating a binary-coded spread sequence arriving at a frequency f and having m bits with a locally generated spread sequence by phase-shifting a multiplicity of locally generated spread sequences with respect to the received spread sequence;

correlating the received spread sequence with a locally generated spread sequence at said frequency f;

storing the received spread sequence and processing the stored, received spread sequence at said oversampling rate equal to i*f, where i is an integer; and

splitting the stored, received spread sequence into i sections and carrying out the correlation in i steps.

5. The correlator according to claim 4, wherein said comparator has a comparator output, and including an adder comprising two-bit adders configured to form a cascaded interconnection, each of said two-bit adders having at least two inputs and an output, said output of each of said two-bit adders connected to one of said at least two inputs of a succeeding one of said two-bit adders, said adder connected to said comparator output and configured to add up logic values produced during bit-by-bit comparison for matching bit positions.